AF/2614 IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Group Art Unit: 2614
Examiner: Paulos M. Natnael

In Re PATENT APPLICATION Of:

Applicant(s)	:	Yasunori SATOH	)
Serial No.	:	09/880,090	) **APPEAL BRIEF**
Filed	:	June 14, 2001	)
For	:	VIDEO SIGNAL CONTROL CIRCUIT	)
Attorney Ref.	:	OKI 276	)

June 20, 2005

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450
Mail Stop Appeal Brief - Patents

Sir:

INTRODUCTION

This is an Appeal to the Board of Patent Appeals and Interferences from the decision, in the Office Action dated December 14, 2004, finally rejecting claims 1, 2, 4 and 16 of the above-referenced application. A Notice of Appeal was timely filed with a Petition for Extension of Time, and the applicable fees, on April 19, 2005.

(i) REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Oki Electric Industry Co., Ltd.

(ii) RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of the undersigned attorney, there are no prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the present appeal.

(iii) STATUS OF CLAIMS

Claims 1, 2, 4-7 and 10-18 are pending in this application. Claims 6, 7, 10-15, 17 and 18 have been allowed. Claim 5 is objected to, but would be allowable if rewritten to include all the limitations of the base claim and any intervening claims. Claims 1, 2, 4 and 16 stand finally rejected and are under appeal.

(iv) STATUS OF AMENDMENTS

Amendments were filed on January 26, 2004 and July 7, 2004, and both amendments have been entered. A Request for Reconsideration was filed on February 14, 2005 in response to the final Office Action dated December 14, 2004. An Advisory Action dated April 4, 2005 maintained the finality of the rejection of claims 1, 2, 4 and 16.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The present application is directed to a video signal control circuit that receives a video signal obtained by decoding a composite video signal from a VTR (video tape recorder) or the like, and regulates the outputted video signal such that the number of

pixels (pixel number) in each line of the video signal is constant (application page 1, lines 9-12). As disclosed in Figure 1 of the application's drawings, a delay circuit 10 receives an input data 100 whose pixel number per one line is uneven (i.e., a non-standard signal). The delay circuit 10 passes the input data 100 through the delay elements to thereby generate plural data whose delays are different from each other by one clock period. The delay circuit 10 may, for example, be configured as an n-stage flip-flop (FF). The delay circuit 10 sequentially transfers the input data 100 through the n-stage FF in accordance with a system clock 104 (not illustrated) of the video decoder. Thereby, the delay circuit 10 generates data 110-0 ~ 110-n each having a delay that differs by one clock period. The input of the delay circuit 10 and the outputs of each FF are each connected to a selector circuit 14, so that the data 110-0 ~ 110-n are inputted to the selector circuit 14 (page 6, lines 8-22).

A counter 12 counts the pixel number per one line of the input data 100. The counter 12 is reset by a horizontal synchronous signal 102 from the video decoder to start counting the clock 104. The counter 12 counts the number of the clock 104 that is inputted during the period of one line to generate a discrete value signal 106 that is inputted to the selector circuit 14 (page 7, lines 4-13).

The selector circuit 14 includes a judgment circuit 140 and a selector 142. The selector circuit 14 inputs the discrete value signal 106 to the judgment circuit 140, and inputs the data 110-0 ~ 110-n from the FF circuit 10 to the selector 142. The judgment circuit 140, receiving the discrete value signal 106 from the counter 12, subtracts the pixel number indicated by the discrete value signal 106 from the standard pixel number held by in a first memory register, and calculates the difference. A delay corresponding

to the calculated difference, expressed in terms of clock periods, is added to a selected initial delay held in a second memory register, and the judgment circuit 140 generates a control signal 108 indicating the updated delay, and delivers it to the selector 142 (page 7, line 14 to page 8, line 5).

The selector 142 selects the data having the delay that the control signal 108 from the judgment circuit 140 indicates out of the data 110-0 ~ 110-n inputted from the FF circuit 10, and outputs the result as an output data 112. Further, a vertical synchronous signal 114 is inputted to the reset terminal of the selector 142, so that the selector 142 is initialized each field by this vertical synchronous signal 114. Accompanied with this initialization, the delay of the FF circuit 10 is returned to the initial setting (page 8, lines 6-20).

In the case of a field in which the lines are being continuously inputted whose pixel number per one line is different from the standard pixel number, and the pixel number per one line is consistently smaller than the standard pixel number, the delay of the data selected by the selector 142 becomes gradually larger. On the other hand, when the pixel number per one line is consistently larger than the standard pixel number, the delay of the data selected by the selector 142 becomes gradually smaller. The extent to which the pixel dispersion can be absorbed depends upon the number n of the FF stages in the FF circuit 10, which determines the maximum delay of the data generated by the FF circuit 10. However, as noted above, the foregoing processing is initialized each field by the vertical synchronous signal 114, and the delay of the FF circuit 10 is returned to the initial setting (page 10, line 22 to page 11, line 7).

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 4 and 16 stand rejected under 35 U.S.C. §102(b) as being anticipated by Watson, US Patent No. 5,034,814. Claim 2 stands rejected under 35 U.S.C. §103(a) as being obvious over the Watson reference. Claims 1, 2, 4 and 16 are set forth in the claims appendix to this Brief in their currently amended form.

(vii) ARGUMENT

The Rejection for Anticipation by Watson

The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the examiner. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

Anticipation, under 35 U.S.C. §102, requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Although anticipation requires only that the claim under attack "read on" something disclosed in the references, all limitations of the claim must be found in the reference, or "fully met" by it. See Kalman v. Kimberly-Clark Corp., 71 to 3 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983).

The Watson reference cited by the Examiner is directed to a system for converting a high definition video signal corresponding to a high-definition picture, into a sub-sampled video signal compatible with NTSC transmission by outputting the NTSC samples in a manner which preserves in the NTSC signal the relative frame-to-frame geometric offsets used in the sampling process, thereby minimizing NTSC flicker

on conventional NTSC receivers (see Abstract).

Independent Claim 1 and Dependent Claims 4 and 16

Independent claim 1 recites a video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising: a delay circuit delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data; a counter circuit that counts a pixel number of each line in the input data; and a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and outputs a calculated difference signal; and a selector combining the delayed input data in response to the calculated difference signal to generate as an output data, combined input data having the standard number of pixels.

In the Final Action, the Examiner asserts Watson discloses all of the claimed subject matter. The Appellant respectfully disagrees.

For example, the Examiner points to the counter 132 in Figure 21 of Watson as corresponding to the counter circuit recited in claim 1. In Watson, the counter 132 receives an output of a pixel rate clock 130 that is provided with an HD sync signal (see column 15, lines 10-11). The HD sync signal is separated from a composite HD video signal and is used for locking the pixel rate clock to the HD signal frame rate (see column 15, lines 11-13). Therefore, the counter 132 cannot count a pixel number of each line in the input data, as claim 1 requires, because the HD video signal itself is not applied to the counter 132. The counter 132 in Watson is shown in Figure 21 as a simple divide-by-two counter and clearly has a very different function from that of the counter circuit of

claim 1.

In addition, the Examiner points to the switch control circuit 49′ in Figure 21 of Watson as corresponding to the judgment circuit recited in claim 1. Since the switch control circuit 49′ is connected to the pixel rate clock 130, the switch control circuit may respond to a pixel number generated by the pixel rate clock 130. However, as discussed above, the pixel rate clock 130 does not receive the input data, but receives only the HD sync signal. Therefore, the switch control circuit 49′ cannot calculate the difference between a standard number of pixels in a line and the pixel number counted by the counter circuit, as claim 1 requires. That is, the switch control circuit 49′ is clearly different from the judgment circuit of claim 1.

Further, the Examiner points to the switch 51 in Figure 21 of Watson as corresponding to the selector recited in claim 1. But, the switch 51 simply switches between first and second positions so as to select different delays and attenuations to apply to the inputted HD signal data (see, for example, column 12, a line 63-67). The switch 51 cannot combine the delayed input data to generate as an output data, combined input data having the standard number of pixels, as claim 1 requires. Therefore, the switch 51 is clearly different from the selector of claim 1.

To summarize, Watson discloses that the counter 132 receives the output of the pixel rate clock 130 and the reset signal from the HD sync separator 47′ and controls the output switch 51 via the switch control circuit 49′ so that processing is applied to those pixels with vertical offset but is not applied to those with no vertical offset (see column 15, lines 11-17). The purpose of the circuit shown in Figure 21 of Watson is to carry out a vertical sub-sampling method on the pixels in different scan lines of an HD video signal

so as to generate an NTSC signal (see column 15, lines 3-5). On the other hand, the claimed invention has a very different function and purpose, namely, to generate an output video data that has a standard number of pixels in each scan line by selectively combining delayed versions of the same input scan line data. As discussed above, the elements of the claimed invention are correspondingly different from those of the prior art reference. Thus, is respectfully submitted that claim 1 is not anticipated by the applied prior art.

Dependent claims 4 and 16 recite additional limitations to further define the invention. They are therefore patentable for at least the reason that they depend from claim 1.

The Rejection for Obviousness Over Watson

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). It also is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). In so doing, the Examiner is required to make the factual determinations set forth in Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 148 USPQ 459 (1966), and to provide a reason why one having ordinary skill in the art would have been led to modify the prior art reference to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). Such a reason

must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.d 281, 227 USPQ 657 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983).

In determining obviousness, the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Harkness Int'l. Inc. v. Simplimatic Eng'g. Co., it 819 F.2d 1100, 2USPQ2d 1826 (Fed. Cir. 1987). The Examiner must give adequate consideration to the particular problems and solution addressed by the claimed invention. Northern Telecom Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); In re Rothermel, 276 F.2d 393, 125 USPQ 328 (CCPA 1960).

The issue is not whether it is within the skill of the artisan to make the proposed modification but, rather, whether a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so. The fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggestions the desirability of the modification. See In re Keller, 642 F.2d 413, 208 USPQ 817 (CCPA 1981), In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Dependent Claim 2

Dependent claim 2 recites that the delay circuit includes a plurality of flip-flop circuits converting the input data into the delayed input data with each delayed by one clock. Regarding claim 2, the Examiner takes official notice that it is notoriously well known in the art to construct a delay circuit from a plurality of flip-flops, and therefore it would have been obvious to one skilled in the art at the time the invention was made to modify the system of Watson by providing a plurality of flip-flop circuits in order to utilize a reliable circuit and cut the cost of the overall system as well. The Applicant respectfully submits that the modification suggested by the Examiner does not overcome the other deficiencies in the base reference discussed above. Thus, even if the modification proposed by the Examiner were suggested by the prior art (which the Applicant does not admit), the application of the modification to Watson would not yield the claimed invention.

Further, the Examiner's argument appears to ignore the express requirement of claim 2 that the delay circuit convert the input data into a plurality of delayed input data with each delayed by one clock period. Rather, what is disclosed in Fig. 21 of Watson, upon which the Examiner relies, are two ½ line delays (53,55). These may be appropriate to the sub-sampling function being performed in Watson, but clearly not applicable to the present invention.

CONCLUSION

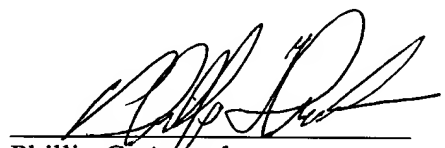
In summary, it is respectfully submitted that the Examiner (i) has failed to apply art which teaches or suggests, the claimed invention, (ii) has applied art in a manner

inconsistent with its teachings, and (iii) has, in general, failed to establish a prima facie case for the rejection. The applied art does not provide any teaching, or suggestion within its teachings, which would lead to the features or advantages of the instant invention discussed above, and that for at least these reasons the appealed claims patentably define over the art.

Thus, it is submitted that the rejection of claims 1, 4 and 16 under 35 U.S.C. §102(b) as being anticipated by Watson, US Patent No. 5,034,814, and the rejection of claim 2 under 35 U.S.C. §103(a) as being obvious over Watson, are in error and reversal is clearly in order and is courteously solicited.

The Appeal Brief fee of $500 is included in a remittance that is being submitted concurrently. Should this remittance be accidentally missing or insufficient in amount, or should additional fees be required, please charge any deficiency to our Deposit Account No. 18-0002 and notify the undersigned attorney accordingly.

Respectfully submitted,



Phillip G. Avruch
Registration No. 46,076
Customer No. 23995
(202) 371-8976
(202) 408-0924 (facsimile)

(viii) Claims Appendix

The following claims are under appeal:

1. A video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising:

a delay circuit delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and outputs a calculated difference signal; and

a selector combining the delayed input data in response to the calculated difference signal to generate as an output data, combined input data having the standard number of pixels.

2. A video signal control circuit as claimed in Claim 1, wherein the delay circuit includes a plurality of flip-flop circuits converting the input data into the delayed input data with each delayed by one clock.

4. (Original) A video signal control circuit as claimed in Claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal.

16. A video signal control circuit as claimed in Claim 1, wherein the counter circuit counts the pixel number of each line in the input data in response to a horizontal synchronous signal received by the counter circuit.

(ix) Evidence Appendix

No new evidence is being submitted with this Brief.

(x) Related Proceedings Appendix

In view of section (ii) of this Brief, no copies of decisions are appended.